NONVOLATILE SEMICONDUCTOR MEMORY DEVICE WITH A FAIL BIT DETECTING SCHEME AND METHOD FOR COUNTING THE NUMBER OF FAIL BITS

This application relies for priority upon Korean Patent Application No. 2000-73031, filed on December 4, 2000, the contents of which are herein incorporated by reference in their entirety.

Field of the Invention

The present invention relates to an integrated circuit devices, and more particularly to an electrically erasable and programmable nonvolatile semiconductor memory device for use in electronic devices.

Background of the Invention

An electrically erasable and programmable nonvolatile semiconductor memory device is used for storing data in electronic systems. Such systems are typically equipped with an error correction code algorithm, as is well known in the art. If an error is generated in the system, it can be corrected via the error code algorithm, even though the error may be generated in a reading or writing operation of the nonvolatile semiconductor memory device. That is to say, the electronic system, which is equipped with the error correction code algorithm, allows containing the number of amendable fail bits.

The nonvolatile semiconductor memory device, in particular, NAND type flash memory device comprises an array consisting of plurality of array or memory blocks. In general, every manufactured memory array includes allowable bad blocks, which are not substantially used.

A test operation is performed on the packaged or completed NAND type flash memory device before this memory device is loaded. When the test operation is performed, such memory device should be discarded if it is determined that at least one of normal array blocks of the array have fail bit(s).

More particularly, if the number of fail bits of the array block found in the test operation does not exceed the number of amendable fail bits of the electronic system, the NAND type flash memory device having a bad block determined in the test operation can be

used in the electronic system which is equipped with the error correction code algorithm. By keeping more of the manufactured memory devices, the yield can be improved.

There are a number of ways of testing the manufactured memory devices. Many packaged memory devices can be tested concurrently, to reduce testing time. Then, as the error capturing RAM of the test device simultaneously testing the packaged memory devices is limited, a total test result is stored in the error capture RAM of the test device. According to this test scheme, such an array block is determined as a bad block, if at least one bit is failed in each array block of the respective packaged memory device. The problem with this technique is that it is impossible to verify the number of fail bits in the array block determined as the bad block.

In another way of testing, the fail bits are counted one by one in each test process by using software. That is, the exact number of fail bits of each memory device can be counted by storing the test result corresponding to every memory cells to the error capture RAM of the test device. The problem, however, with such a software scheme is that, as the error capture RAM of the test device is limited, the number of the memory devices that can be tested simultaneously is reduced. This means that overall test time must be increased.

A need remains for determining exactly the number of fail bits of the memory device accepted in the electronic system, so that the memory device determined as a bad chip in a test operation may be available.

Summary of the Invention

It is, therefore, an object of the present invention to provide a nonvolatile semiconductor memory device that can count the number of fail bits generated in one of its array blocks.

It is another object of the invention to provide a method for counting the number of fail bits generated in an array block of the nonvolatile semiconductor memory device.

It is still another object of the invention to provide a nonvolatile semiconductor memory device that can be tested in reduced time, and a testing method thereof.

It is further still another object of the invention to provide a nonvolatile semiconductor memory device with improved yield, and a testing method thereof.

In order to attain the above objects, the present invention provides semiconductor memory devices and methods for determining exactly the number of their own fail bits.

A nonvolatile semiconductor memory device according to an embodiment of the invention has a special circuitry for counting its own fail bits in a special test mode. During

the test mode, test data is stored in the memory, and also in a special expected data buffer. The test data stored in the memory cells are then compared to that stored in the expected data buffer. Where they do not correspond, that is registered as detected fail bits.

The nonvolatile semiconductor memory device can count exactly the number of fail bits generated in the process of programming/reading the data in/from the memory device by the method thereof.

The invention gives the advantage of improving the yield by exactly counting the number of fail bits generated in the process of programming/reading the data in/from the memory device.

The present invention will be better understood from the following detailed description of the exemplary embodiment thereof taken in conjunction with the accompanying drawings, and its scope will be pointed out in the appended claims.

Brief Description of the Drawings

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

Figure 1 is a block diagram illustrating a nonvolatile semiconductor memory device according to first embodiment of the present invention;

Figure 2 shows a preferred embodiment of an expected data input buffer block shown in Figure 1;

Figure 3 shows a preferred embodiment of a fail bit detecting block shown in Figure 1;

Figure 4 shows a preferred embodiment of a fail bit counter and latch block shown in Figure 1;

Figure 5 shows a preferred embodiment of a T flip-flop shown in Figure 4;

Figure 6 is a view illustrating a wave relation of the input signals and the output signals of Figure 4;

Figure 7 shows a preferred embodiment of a data output buffer block shown in Figure 1;

Figure 8 shows a preferred embodiment of a read-out enable buffer in a global buffer and control buffer block shown in Figure 1;

Figure 9 is a flow chart illustrating an overall operation of the nonvolatile semiconductor memory device according to the present invention;

Figure 10 is a flow chart explaining the fail bit detecting operation according to the present invention;

Figures 11A and 11B are timing diagrams of the operation of the nonvolatile semiconductor memory device in which 2 or more fail bits are generated;

Figure 12 is a timing diagram of the operation of the nonvolatile semiconductor memory device in which one fail bit is generated;

Figure 13 is a timing diagram of the operation of the nonvolatile semiconductor memory device in which no fail bit is generated;

Figure 14 is a block diagram of a nonvolatile semiconductor memory device according to a second embodiment of the present invention;

Figure 15 shows a preferred embodiment of a data output buffer block shown in Figure 14; and

Figure 16 shows a preferred embodiment of a fail bit detecting block shown in Figure 14.

Figure 17 is a flowchart illustrating a method according to a general embodiment of the present invention.

Description of the Preferred Embodiment

The following detailed description is of the best modes for practicing the invention. It should be understood that the description of these preferred embodiments is merely illustrative, and that other embodiments are possible. Accordingly, the presented embodiments should not be taken in a limiting sense for the invention.

Figure 1 is a block diagram showing a nonvolatile semiconductor memory device according to first embodiment of the present invention.

Referring first to Figure 1, a NAND type flash memory device 1 of a nonvolatile semiconductor memory device comprises an array 100 as a device for storing data. The array 100 comprising a plurality of memory cells arranged in the form of a matrix having rows or wordlines, and columns or bitlines, not shown in the figure. Each memory cell includes an electrically erasable and programmable ROM cell transistor.

The nonvolatile semiconductor memory device 1 comprises a global buffer and control buffer block 110, a command register block 120, a row address buffer and decoder block 130, a column address buffer and decoder block 140, a row decoder block 150, a page buffer and latch block 160, a column select block 170, and a data input/output control block 180.

The global buffer and control buffer block 110 includes a plurality of control buffers for buffering control signals CLE, ALE, nCE, nRE, nWE supplied from the outside and global buffers for receiving addresses or data supplied via input pins IOi (i=0~7). In the embodiment of Fig. 1, the signals applied to the input/output pins IOi are used as addresses, data, or commands according to a combination of the control signals.

When the combination of the control signals inputted currently represents, for example, a command input, the signals CMD[i] inputted to input/output pins IOi are passed to the command register block 120. And, when the combination of the control signals inputted currently represents, for example, an address input, then the signals XAD[i], XAD[i] outputted from the global buffer and control buffer block 110 are passed to the row address buffer and decoder block 130 and the column address buffer and decoder block 140, respectively. When the combination of the control signals inputted currently represents, for example, a data input, the signal Data[i] outputted from the global buffer and control buffer block 110 according to the signals inputted to input/output pins IOi are passed to the data input/output control block 180.

Continuing to refer to Figure 1, the command register block 120 generates a fail bit detecting command signal FD or a fail bit read-out command signal FR in response to the signals CMD[i] supplied from the global buffer and command buffer block 110. The row decoder block 150 selects a word line in the memory block selected in the array 100 in response to the address XAD[n:0] supplied from the row address buffer and decoder block 130. During a reading operation, the page buffer and latch block 160 detects and amplifies the data stored in the memory cells related to a selected word line or selected page of the selected memory block and stores the detected data temporally.

During a programming or writing operation, the page buffer and latch block 160 latches the supplied write data temporarily by means of the global buffer and control buffer block 110, the data input/output control block 180, and the column select block 170.

During a reading operation, the column select block 170 selects some of the read-out data bits, for example, the data bits corresponding to input/output pins, which correspond to a page and which is latched in the page buffer and latch block 160, in response to the address signals Yad[m:0] supplied from the column address buffer and decoder block 140, and passes the selected read-out data bits to the data input/output control block 180.

The nonvolatile semiconductor memory device 1 of the present invention further comprises an expected data input buffer block 190, a fail bit detecting block 200, a fail bit counter and latch block 210, and a data output buffer block 220, as is shown in Fig 1. The

expected data input buffer block 190 operates in response to a fail bit detecting command signal FD from the command register block 120 and outputs the expected data bits DEX[i] according to input/output pins IOi.

The point of testing is by having the expected data bits DEX[i] be identical with the data bits programmed in the array 100. This way, if there is a fail bit, it may output something different than programmed.

Testing is accomplished during a test operating mode. During the test operating mode, fail bit detecting command signal FD is activated.

A preferred embodiment of the expected data input buffer block 190 according to the present invention is shown in Figure 2. While the expected data input buffer corresponding to only one input/output pin is shown in Figure 2, it is apparent that the buffers corresponding to the rest of the input/output pins also have the same structure. The expected data input buffer 190 is comprised of a 2-input NAND gate 501 and an inverter 502. The NAND gate 501 includes first input terminal connected to the corresponding input/output pin IO[i] and second input terminal for receiving the fail bit detecting command signal FD and then the inverter 502 receives the output of the NAND gate 501 and outputs the expected data bit DEX [i].

Continuing to refer to Figure 1, the fail bit detecting block 200 operates in response to the fail bit detecting command signal FD and receives the read-out data bits DS[i] selected by the column select block 170 in accordance with the read-out enable signal nREO and the fail bit detecting command signal FD. The read-out enable signal nREO can be generated by combination of the signals nRE and nCE by means of logic gates.

Referring briefly to Figure 8, according to one embodiment, the read-out enable signal nREO is formed by combining signals nRE and nCE through a NOR gate 584 and an inverter 585.

Referring back to Figure 1, the fail bit detecting block 200 determines whether inputted read-out data bits DS[i] each match the expected data bits DEX[i] inputted from the expected data input buffer block 190 or have fail bit(s). The fail bit detecting block 200 generates fail flag signal FF[0] or FF[1] according to the determination result. A preferred embodiment of the fail bit detecting block 200 according to the present invention is shown in Figure 3.

Referring next to Figure 3, the fail bit detecting block 200 includes a number of input parts 200a, each corresponding to inputted read-out data bits DS[7]~DS[0], and a fail flag signal generating part 200b. Only one of the input parts is shown in Figure 3, as the rest of them are preferably implemented with the same structure.

Input part 200a outputs the corresponding read-out data bits DS[i] in response to the signal FD and nREO as an internal read-out data bit DSI[i]. Input part 200a includes inverters 503, 508, 509, and 511, two PMOS transistors 504 and 505, two NMOS transistors 506 and 507, and a NAND gate 510, which are connected between them as is shown in the figure.

During a normal operation of memory 1, the fail bit detecting command signal FD is maintained at a low level. Then the internal read-out data bit DSI[i] is also maintained at a low level, without regard to a value of the corresponding read-out data bit DS[i], or a logic level of the read enable signal nREO.

During a test mode, the fail bit detecting command signal FD is activated to go to a high level. Then the value of the corresponding internal read-out data bit DSI[i] depends upon the value of the read-out data bit DS[i] inputted during the read enable signal nREO is in a low level.

Continuing to refer to Figure 3, the fail flag signal generating part 200b compares the internal read-out data bits DSI[i] outputted from the input parts 200a with the corresponding expected data bits DEX[i] outputted from the expected data input buffer 190. The fail flag signal generating part 200b outputs the fail flag signals FF[0] and FF[1] according to the comparison result during the read enable signal nREO is in a low level.

If one of the internal read-out data bits DSI[i], for example, DSI[7] is, for example, a fail bit, that is to say, if the internal read-out data bit DSI[7] does not match the expected data bit DEX[7], the output of a XOR gate 512 becomes "1" and the outputs of the rest of XOR gates 513~515 and 516~519 become "0". According to such condition, when the read-out enable signal nREO goes to a low level, a NOR gate 548 outputs a fail flag signal FF[0] having a low to high transition and the output of the NOR gate 549, FF[1] is maintained in the initial low level. Consequently, if one of the internal read-out data bits is a fail bit, the fail flag signal FF[0] is activated in the form of at least one pulse.

If the internal read-out data bits DSI[7] and DSI[0] are fail bits, the outputs of the XOR gates 512 and 519 become "1" and the outputs of the rest of XOR gates become "0". According to such condition, during the read-out enable signal nREO is in a low level, NOR gates 548 and 549 output fail flag signals FF[0] and FF[1] having a low to high transition, respectively. Consequently, if at least two of the internal read-out data bits are fail bits, the fail flag signals FF[0] and FF[1] are activated in the form of at least one pulse.

Referring back to Figure 1, the fail bit counter and latch block 210 is initialized when the fail bit detecting command signal FD is transitioned from a low level to a high level. The

fail bit counter and latch block 210 counts the number of fail bits in response to the fail flag signals FF[0] and FF[1] outputted from the fail bit detecting block 200 and outputs fail status signals FS [i] as fail codes representing the counted number of fail bits. A preferred embodiment of the fail bit counter and latch block 210 is shown in Figure 4.

As is shown in Figure 4, the fail bit counter and latch block 210 includes a pulse generator 560, two T flip-flops 561 and 562, a NOR gate 563, an inverter 564, and S-R flip-flops 565 and 566, which are connected between them as is shown in the figure. The T flip-flops 561 and 562 operate as counters, whereas the S-R flip-flops 565 and 566 operate as latches. A preferred embodiment of the T flip-flop is shown in Figure 5. The pulse generator 560 generates a pulse signal CLR in response to the fail bit detecting command signal FD having a low to high transition. The T flip-flops 561 and 562 and the S-R flip-flops 565 and 566 are initialized by the pulse signal CLR. The fail bit counter and latch block 210 operates depending upon the number of fail bits as below.

If the number of fail bits is two or more, the fail bit counter and latch block 210 operates as follows. After becoming initialized, when the fail flag signal FF[0] has a low to high transition, the output Q of the T flip-flop 561 has a low to high transition thereby causing the output FS[0] of a S-R flip-flop 565 to have a low to high transition as is shown in Figure 6. And then if the fail flag signal FF[0] has a low to high transition again, the output Q of the T flip-flop 562 has a low to high transition thereby causing the output of a NOR gate 563 to have a high level regardless of a logic level of the fail flag signal FF[1]. Consequently, the output FF[1] of the S-R flip-flop 566 has a low to high transition as is shown in Figure 6.

Furthermore, when fail flag signals FF0 and FF1 have a low to high transitions at the same time, as is shown in Figure 6, the S-R flip-flop 565 outputs a fail status signal FS0 in a high level according to an output of the T flip-flop 561, while the S-R flip-flop 566 outputs a fail status signal FS1 in a high level according to a fail flag signal FF1 in a high level supplied via a NOR gate 563 and an inverter 564.

If the number of fail bits is only one, the operation of the fail bit counter and latch block 210 is as follows. After initialized, when a fail flag signal FF[0] has a low to high transition, the output Q of the T flip-flop 561 has a low to high transition thereby causing the output FS[0] of a S-R flip-flop 565 to have a low to high transition, as is shown in Figure 6. If there is no fail bit, fail bit signals FS[0] and FS[1] outputted from the fail bit counter and latch block 210 are maintained at a low level as is shown in Figure 6.

Still referring to Figure 1, a key feature of the first embodiment of the invention is that detecting, and also counting, the fail bits occurs before the data output buffer block 220.

A normal output data path is provided from memory cell array 100 to data output buffer block 220. During a normal read-out operation mode, the data output buffer block 220 delivers read-out data bits DS[i] outputted from the data input/output control block 180 to the corresponding input/output pins IO[i], through the normal data output path.

Detecting, and also counting the fail bits takes place by diverting from the normal output data path. During a test operation mode for detecting and counting the fail bits, the normal data output path of the data output buffer block 220 is blocked. Fail status signals FS[i] (i=0~7) outputted from the fail bit counter and latch block 210 are outputted by the activation of the fail bit read-out command signal FR.

Referring to Figure 7 illustrating a preferred embodiment of the data output buffer block 220, when the signals FR and FD are maintained at a low level, the normal data output path is formed via a transfer gate 574. On the other hand, when the fail bit read-out command signal FR is maintained at a high level, the normal data output path is blocked by the path gate 574, while the fail status signal FS [i] is outputted to the corresponding input/output pin IO[i] via the transfer gate 578.

The fail status signals FS [i] outputted from the fail bit counter and latch block 210 correspond to the input/output pins IO [i], respectively. In this embodiment, because there is used with only two fail status signals FS[0] and FS[1], the rest of the fail status signals FS[2]~FS[7] will be set to be maintained at a low level.

Referring now to Fig. 17, a flowchart 1700 is used to illustrate a general method according to an embodiment of the invention. The method of flowchart 1700 may also be practiced by a device made according to the invention.

According to an optional box 1710, a fail bit detecting command signal is received. This results in placing a device in a test mode.

According to an optional next box 1720, a counter is initialized. This may be performed as a result of receiving the fail bit detecting command signal.

According to a next box 1730, test data is stored in memory cells of the device. If the bits are not fail bits, then the test data will be stored properly.

According to a next box 1740, expected data is input in an expected data buffer of the device. Preferably, the expected data is identical to the test data.

According to a next box 1750, the stored expected data is compared with the stored test data. This will reveal whether the test data was stored properly. If not, it will be inferred that this was a fail bit.

According to a next box 1760, failure occasions are registered in a register of the device. Failure occasions are instances in which the inputted expected data does not correspond with the compared outputted expected data. These are deemed to have occurred due to the presence of fail bits.

According to an optional next box 1770, the registered failure occasions are counted in a counter of the device.

According to an optional next box 1780, signals are output to an output data buffer of the device. The signals encode a number of the counted failure occasions. This way the number of failed bits is inferred.

A number of variations are possible from the above described method. An example is seen below.

Referring now to Figure 9, a flow chart illustrates the overall operation of the nonvolatile semiconductor memory device 1 of Figure 1. After a data input command is inputted in step S100, a row address and then a column address to be tested are sequentially inputted in step S110. And then a data to be programmed is sequentially inputted via input/output pins IO[i] in step S120. After the preparation for executing a program is completed, a programming operation is performed according to the input of a program executing command in step S130. If a status reading command is inputted in step S140, it is determined whether the chip is ready or busy, in step S150. If the chip is ready, it is determined whether the programming operation has been normally performed in step S160. If the chip is not ready, the programming operation is ended as a fail. If the programming operation has been normally performed, the programming operation will be ended as a pass.

The above described portion of the programming method is also disclosed in U.S. patent No. 5,473,563, U.S. patent No. 5,541, 879, U.S. patent No. 5,546,341, and U.S. patent No. 5,712,818, which are hereby incorporated in this document by reference.

If the programming operation is determined as a pass in step S160, a read-out command is inputted in step S170 and a row address and a column address are inputted in step S 180. Then a value of the column address is set to a minimum (LSB). Then, cell data stored in memory cells of a row or a page corresponding to the set row address are sensed by the page buffer and latch block 160 in step S190. In next step S200 the fail bit detecting command is inputted and the number of fail bits is detected and stored via a series of fail bit detecting procedure in step S210. The fail bit condition read-out command is inputted in step S220, a fail code is outputted representing the number of fail bits in step S230. The fail bit detecting steps S200 to S230 described above will be discussed more in detail hereinafter.

The flow chart illustrating the operation of detecting fail bits according to the invention is shown in Figure 10. Figures 11A and 11B are diagrams of an operational timing of a nonvolatile semiconductor memory device in which 2 or more fail bits are generated. Fail bit detecting operation will be discussed with reference to appended drawings as follows.

For convenient description, it is assumed that a programming operation is being performed and a read command is being inputted over a page. That is to say, the fail bit detecting operation over one page will be described next. However, it is apparent to a person skilled in the art that the number of fail bits contained in a memory block including a plurality of pages can be detected by a fail bit detecting scheme according to the invention.

As is shown in Figure 10, the fail bit detecting command is sent to the command register block 120 via the global buffer and control buffer block 110. The command register block 120 activates a fail bit detecting command signal FD in response to a fail bit detecting command. According to activation of the fail bit detecting command signal FD, the pulse generator 560 of the fail bit counter and latch block 210 generates a pulse signal CLR (see Figure 4). Consequently, T flip-flops 561 and 562 and S-R flip-flops 565 and 566 of the fail bit counter and latch block 210 are initialized. These initialized operations are performed in step S310. Then, the fail status signals FS [0]-FS[7] are maintained at a low level, as is shown in Figures 11A and 11B.

After the column address is set to a minimum LSB in next step S320, it is determined whether the column address is a maximum MSB in step S330. The column select block 170 selects data bits corresponding to the column address set to the LSB among data bits sensed by a reading operation and sends the selected read-out data bits to the fail bit detecting block 200 via the data input/output control block 180 in synchronization with the read enable signal nREO. Furthermore, the expected data buffer block 190 sends to the fail bit detecting block 200 the expected data bits DEX [i] which are supplied to the input/output pins IO [i] during an activation period of the fail bit detecting command signal FD.

The fail bit detecting block 200 compares the inputted read-out data bits DSI [i] with the expected data bits DEX [i] and generates the fail flag signals FF[0] and FF[1] according to the comparison result. It is determined whether the fail bits are generated in the next step S350. For example, if one of the read data bits is a fail bit as is shown in Figure 11A, the fail flag signal FF[0] is activated during a low period of the read-out enable signal nREO thereby causing the fail status signal FS[0] to be activated to a high level as is described above. That is to say, the number, 1, meaning that 1-bit fail is generated is stored in a S-R flip-flop 565 of the fail bit counter and latch block 210 in step S360. Then, the process proceeds to step S370

in which the column address is incremented in synchronization with the signal nRE. If the read-out data bits match all the expected data bits, the process proceeds to step S370.

The loop of the steps S330 to S370 is repeatedly performed until the column address reaches a maximum. When the loop of the steps S330 to S370 is performed, one of the read-out data bits may be determined as a fail bit back, as is shown in Figure 11A. In this case, the fail flag signal FF[1] is activated during a low period of the read-out enable signal nREO to thereby causing the fail status signal FS [1] to be activated to a high level as is discussed above. That is to say, the number, 2, meaning that 2-bit fails are generated is stored in S-R flip-flops 565 and 566 of the fail bit counter and latch block 210.

Also as is shown in Figure 11B, 2 data bits of the read-out data bits can be determined as fail bits simultaneously. In this case, the fail flag signals FF[0] and FF[1] are activated simultaneously during a low period of the read-out enable signal nREO to thereby causing the fail status signals FS[0] and FS[1] to be activated to a high level simultaneously. That is to say, the number, 2, meaning that 2-bit fails are generated is stored in S-R flip-flops 565 and 566 of the fail bit counter and latch block 210.

Sequentially, if it is determined that the column address is a maximum MSB in step S330, the fail bit status read-out command will be inputted in step S380. According to this a command register block 120 causes the fail bit detecting command signal FD to be at a low level and the fail bit read command signal FR to be at a high level. The data output buffer block 220 outputs the fail status signal FS [0] to FS[7] outputted from the fail bit counter and latch block 210 via the input/output pins IO[0] to IO[7] in response to the fail bit read command signal FR in the high level.

As is described above, since the fail status signals FS[2] to FS[7] are maintained at a low level, the number of fail bits over one page will be determined according to logic statuses of the input/output pins IO[0] and IO[1]. As is known in Figures 11A and 11B, since both the fail status signals FS[0] and FS[1] become at high level, the logic statuses of corresponding input/output pins IO[0] and IO[1] will be "11" ("03h" as a fail code). That is, the fact that 2-bit fails are generated will be detected from the outside.

Referring to Figure 12 illustrating a diagram of the operational timing of the nonvolatile semiconductor memory device in which one fail bit is generated, then as is discussed above, in case only one fail bit is generated, the fail status signal FS[0] is maintained at a high level and the fail status signal FS[1] is maintained at a low level. Since the fail status signals FS[1] and FS[0] are in a high level and a low level respectively, the

logic statuses of the corresponding input/output pins IO[1] and IO[0] will be "01" ("01h" as a fail code). That is, the fact that 1-bit fail is generated will be detected from the outside.

Referring to Figure 13 illustrating a diagram of the operational timing of the nonvolatile semiconductor memory device in which no fail bit is generated, then as is discussed above, in case no fail bit is generated, both the fail status signals FS[0] and FS [1] are maintained at a low level. Since both the fail status signals FS[1] and FS[0] are a low level, the logic statuses of the corresponding input/output pins IO[1] and IO[0] will be "00" ("00h" as a fail code). That is, the fact that no bit fail is generated will be detected from the outside.

According to this fail bit detecting scheme, the number of fail bits of each memory block can be detected. For example, an arbitrary memory block of the memory device after packaged may be determined as a bad block by a progressive fail. Then, if the number of fail bits in the memory block will be in the range of the number of fail bits over which the fail bits can be corrected by an error correction code algorithm of the electronic system, such a memory device can be used as it is without disposal, thereby enhancing the yield of the product.

Figure 14 is a block diagram illustrating a nonvolatile semiconductor memory device 1400 according to the second embodiment of the present invention. The second embodiment of the present invention is identical with the first embodiment of Figure 1 in many aspects, whose identical description is therefore not repeated as superfluous.

A key difference of the second embodiment from the first embodiment is that the sensed data bits DS[i] are sent to a fail bit detecting block 200' via a data output buffer block 220'. In other words, detecting (and also optionally counting) are performed after the data output buffer block 220', not before it. This entails that detection, and also optionally counting, are outside the path between cell array 100 and data output buffer 220'.

Referring to Figure 15 illustrating a data output buffer block 220' according to the second embodiment of the present invention, a data transfer path (including a NAND gate 586 and an inverter 587) for outputting the data bits DS[i] outputted from the data input/output control block 180' as read-out data bits DSI[i] is added to the data output buffer block 220' according to the second embodiment.

Referring to Fig. 16, a fail bit detecting block 200' according to the second embodiment of the invention is shown. It will be recognized that block 200' is similar to the fail flag signal generating part 200b of the fail bit detecting block 200 shown in Figure 3. Its further description is therefore not repeated, as superfluous.

Referring back to Figure 14, the fail bit detecting operation of the nonvolatile semiconductor memory device 1400 is identical with that of first embodiment described with reference to flow charts in Figure 11A and 11B, Figure 12 and Figure 13 and the description thereof will also be omitted. Therefore it will be apparent to a person skilled in the art that the second embodiment has same effects as first embodiment.

As will be described above, the memory device according to the present invention gives enhanced yield of the memory device by exactly counting the number of fail bits generated in the process of programming/reading data in/from a nonvolatile semiconductor memory device. Furthermore, the memory device gives reduced test time over that of a conventional device operated in software.

Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as described in the accompanying claims.